REMARKS

Claims 1-28 are pending in the instant application. Claims 1-28 are rejected. Claims 1, 11 and 20 are amended. No new matter has been added.

103 Rejections

Claims 1-3, 6, 9-13, 16-17, 20-21 and 25-26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dye (U.S. Patent No. 6,173,381) in view of Davis et al. (U.S. Patent No. 4,991,169). The Applicant has reviewed the cited references and respectfully submits that the embodiments of the invention as are recited in Claims 1-3, 6, 9-13, 16-17, 20-21 and 25-26 are neither anticipated nor rendered obvious by Dye (U.S. Patent No. 6,173,381) in view of Davis et al.

The Examiner is respectfully directed to independent Claim 1 which sets forth an embodiment of the present invention that includes a controller chip comprising:

> ...an engine operative to manage a memory, the engine comprising an interface; and a storage element coupled to the engine, the storage element being accessible by a central processing unit (CPU) through the engine, wherein the engine receives commands from the CPU via the interface, manages the storage element via the interface and writes the commands into the memory and wherein the engine incorporates the storage element as part of the memory.

Independent Claims 11 and 20 recite limitations similar to those of Claim 1. Claims 2, 3, 6, 9-10 depend from Claim 1, Claims 12, 13, 16-17 depend from Claim 11, and Claims 21 and 25-26 depend from Claim 20 and set forth further limitations of the claimed invention.

Dye does not anticipate or render obvious a controller chip that includes an engine a memory, and a storage element wherein the engine is operative to manage the memory and wherein "the engine comprises "an interface" as is recited in Claim 1 (independent Claims 11 and 20 contain similar limitations). Moreover, Dye does not anticipate or render obvious a controller chip that includes an engine that "receives commands from the CPU via the interface, and manages the storage element via the interface" as is recited in Claim 1 (independent Claims 11 and 20 contain similar limitations). It should be appreciated that in order to anticipate or render obvious the embodiment of the invention that is set forth in Claim 1 the cited references must teach or suggest, either expressly or inherently, in addition to all of the other limitation of Claim 1, an engine that: (1) includes an interface as a part of the engine; (2) receives commands from a CPU via the interface that is a part of the engine; and (3) manages a storage element via the same interface. The Applicant respectfully submits that such a system structure and operation is neither shown nor suggested by Dye.

Dye discloses a memory controller that includes embedded data compression and decompression engines and that uses data compression to reduce system bottlenecks. However, the system structure that is disclosed by Dye is distinct from that of the system which is set forth in the Applicant's claims and cannot support significant aspects of the functionality of the system that is defined in Applicant's claims. Specifically, Dye does not show a controller engine that comprises an interface with a placement and functionality as is recited in Claim 1.

The actual system design that is disclosed by Dye is shown in Figure 5. Figure 5 of Dye shows an integrated memory controller (IMC) that includes an engine 210 that is coupled to other systems through FIFO buffers 204, 206, 214 and 216. It should be appreciated that engine

210 is coupled to CPU 102 and bus interface logic 202 through FIFO buffers 204 and 206. Dye discloses the following passage at column 13, lines 1-15:

> The bus interface logic 202 couples to an execution engine 210 through two first in first out (FIFO) buffers 204 and 206. In other words, the two FIFO buffers 204 and 206 are coupled between the bus interface logic 202 and the execution engine 210.

The above referenced passage from Dye expressly presents specific structural details of the system that is disclosed by Dye and serves to underscore the structural differences between the system that is disclosed by Dye and the invention that is set forth in Applicant's claims. More specifically, the above referenced passage expressly indicates that bus interface logic 202 is physically separated from execution engine 202 by FIFO buffers 204 and 206.

Despite fundamental differences in the location and role of interface logic 202 disclosed by Dye and the interface that is set forth in Applicant's Claim 1 with respect to other components of their respective systems (as was outlined above), the interface logic 202 disclosed by Dye is nonetheless equated with the recited interface that is set forth in Applicants' Claim 1. However, because of the fundamental differences outlined above, a reading of Dye as teaching or suggesting the embodiment of Applicant's invention as is set forth in Claim 1 that is consonant with basic patent law principles is precluded.

It is important to note that the Dye system employs a mediated (via FIFO buffers) form of communication between the therein disclosed interface logic and engine (which is unlike the system set forth in Applicant's claims where the recited interface is actually a part of the recited

graphics engine - see Applicant's Figure 4). Moreover, commands to the recited storage element are transmitted through the disclosed interface. As such, the graphics engine manages the storage element via the interface that is actually a part of the graphics engine. Nowhere in the Dye reference is there shown a controller chip (graphics) engine that receives commands via an interface and manages a storage element via the interface where the interface is actually a part of the controller chip engine itself as is set forth in Claims 1, 11 and 20. Consequently, the embodiments of the Applicant's invention as are set forth in Claims 1, 11 and 20 are neither anticipated nor rendered obvious by Dye.

Furthermore, the combination of Davis et al. with Dye does not remedy the deficiencies of Dye outlined above. Davis et al. does not anticipate or render obvious a controller chip that includes an engine, a memory, and a storage element wherein the engine is operative to manage the memory and wherein "the engine comprises "an interface" as is recited in Claim 1 (independent Claims 11 and 20 contain similar limitations). Moreover, Dye does not anticipate or render obvious a controller chip that includes an engine that "receives commands from the CPU via the interface, and manages the storage element via the interface" as is recited in Claim 1 (independent Claims 11 and 20 contain similar limitations).

Davis et al. only shows a dual digital signal processor that provides real time links between multiple time division channels of a digital carrier signal. It should be appreciated that the Davis et al. reference is concerned with providing a system that has the capacity to mediate communications between a carrier and a host system. As a result, nowhere in the Davis et al. reference is there shown a controller chip engine that receives commands via an interface and manages a storage element via the interface where the interface is actually a part of the engine

itself as is set forth in Claims 1, 11 and 20. Consequently, the embodiments of the Applicant's invention as are set forth in Claims 1, 11 and 20 are neither anticipated nor rendered obvious by Dye and Davis et al. either alone or in combination.

Therefore, Applicant respectfully submits that Dye and Davis et al. either alone or in combination do not anticipate or render obvious the embodiments of the present claimed invention as are recited in Claims 1, 11 and 20, and as such Claims 1, 11 and 20 are in condition for allowance. Accordingly, Applicant also respectfully submits that Dye and Davis et al. either alone or in combination, do not anticipate or render obvious the embodiments of the present claimed invention as are recited in Claims 2, 3, 6, 9 and 10 dependent on Claim 1, Claims 12, 13 and 16-17 dependent on Claim 11, and Claims 21 and 25-26 dependent on Claim 20, and that Claims 2, 3, 6, 9-10, 12, 13, 16-17, 21 and 25-26 overcomes the basis for rejection under 35 U.S.C. 103(a) as being dependent on allowable base claims.

Claims 4, 5, 7, 8, 14, 15, 18, 19, 22-24, 27 and 28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dye (U.S. Patent No. 6,173,381) in view of Davis et al. (U.S. Patent No. 4,991,169) and further in view of an Official Notice. The Applicant has reviewed the cited references and respectfully submits that embodiments of the present invention as are recited in Claims 4, 5, 7, 8, 14, 15, 18, 19, 22-24, 27 and 28 are neither anticipated nor rendered obvious by Dye (U.S. Patent No. 6,173,381) in view of Davis et al. and further in view of the Official Notice. It should be appreciated that the Official Notice is concerned with the obviousness of utilizing various FIFO buffer geometries but does not address the deficiencies of either Dye or Davis et al. as outlined above. Consequently, the embodiments of the Applicant's invention as set forth in Claims 4, 5, 7, 8, 14, 15, 18, 19, 22-24, 27 and 28 are neither anticipated nor rendered

obvious by Dye in view of Davis et al. and further in view of the Official Notice as these Claims are dependent on base Claims 1, 11 and 20 whose allowability are discussed above.

Conclusion

In light of the above-listed remarks, the Applicant respectfully requests allowance of the remaining Claims.

The Examiner is urged to contact the Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,
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